



Product/Process Change Notice - PCN 18_0190 Rev. -

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This notice is to inform you of a change that will be made to certain ADI products (see Appendix A) that you may have purchased in the last 2 years. **Any inquiries or requests with this PCN (additional data or samples) must be sent to ADI within 30 days of publication date.** ADI contact information is listed below.

PCN Title: ADUCM310/320/320i/322: Metal Edit

Publication Date: 11-Dec-2018

Effectivity Date: 15-Mar-2019 *(the earliest date that a customer could expect to receive changed material)*

Revision Description:

Initial Release

Description Of Change:

The silicon edit involved cutting a single track to disconnect a grounded input to a Test Mux to help power-on Reset conditions.

In some cases this would have prevented the digital LDO from getting a valid bandgap voltage and hence not powering up correctly.

With the silicon edit, the case described above can no longer occur.

Reason For Change:

The edit is required to guarantee a safe VDD ramp rate under all conditions of temperatures and ramp rates.

Impact of the change (positive or negative) on fit, form, function & reliability:

No impact on fit, form, function and reliability

Product Identification *(this section will describe how to identify the changed material)*

Date code changeover to be notified in a future revision of this PCN

Summary of Supporting Information:

Characterization validation has been performed per ADI's standard product correlation procedure. See attached Report.

Supporting Documents

Attachment 1: Type: Test Correlation Report

ADI_PCN_18_0190_Rev_-_ADuCM3xx.pdf

For questions on this PCN, please send an email to the regional contacts below or contact your local ADI sales representatives.

Americas:
PCN_Americas@analog.com

Europe:
PCN_Europe@analog.com

Japan:
PCN_Japan@analog.com

Rest of Asia:
PCN_ROA@analog.com

Appendix A - Affected ADI Models

Added Parts On This Revision - Product Family / Model Number (13)

ADUCM310 / AD90005Z-0	ADUCM310 / AD90005Z-0RL	ADUCM310 / ADUCM310BBCZ	ADUCM310 / ADUCM310BBCZ-RL	ADUCM320 / ADUCM320BBCZ
ADUCM320 / ADUCM320BBCZ-RL	ADUCM320 / ADUCM320BBCZI	ADUCM320 / ADUCM320BBCZI-RL	ADUCM320 / ADUCM320LUM-DIE	ADUCM322 / ADUCM322BBCZ
ADUCM322 / ADUCM322BBCZ-RL	ADUCM322 / ADUCM322BBCZI	ADUCM322 / ADUCM322BBCZI-RL		

Appendix B - Revision History

Rev	Publish Date	Effectivity Date	Rev Description
Rev. -	11-Dec-2018	15-Mar-2019	Initial Release

Analog Devices, Inc.

DocId:4568 Parent DocId:None Layout Rev:7



AHEAD OF WHAT'S POSSIBLE™

ADuCM320/ ADuCM320i ADuCM322/ADuCM322i PCN

11/30/2018

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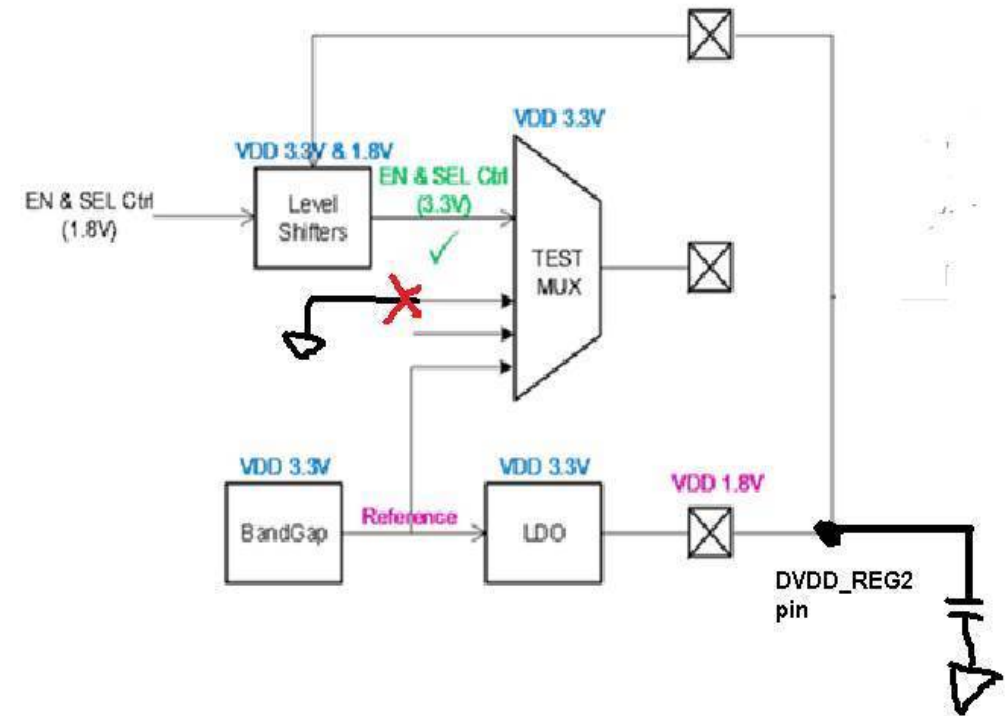


Background for Silicon Iteration

- ▶ A small number of ADuCM32x devices had a Power-up issue
 - Low ppm failure (<10ppm)
 - Failures mainly at low temperatures (<0C) and >50C
 - Failing devices susceptible to Power up problems especially with slow VDD ramp rates
- ▶ Issue identified with digital die 1.8V regulator (LDO)
 - Test screen for old silicon revision identified to provide interim cover
 - But not guaranteed to screen all weak parts.
- ▶ Silicon edit identified to fully fix the issue
 - All revisions of ADuCM310/ADuCM32x fixed
 - Characterization is complete
- ▶ ADI ready to release new revision of ADuCM310/ADuCM32x to production
 - Future shipments will use revised digital die with silicon fix for this issue.

Details on Silicon Change

- ▶ Cut a single track to disconnect a grounded input to a Test Mux – see the red “x” below to indicate the location.
- ▶ When the 3.3V DVDD power supply is rising from 0V towards the Power-On reset threshold voltage, the enable and select signals to the Test MUX shown below are undefined.
- ▶ In some corner cases on previous silicon, this sometimes resulted in the output of the Bandgap being shorted to the GND input of the MUX.
- ▶ This meant that the digital LDO did not get a valid bandgap voltage and did not power up correctly.
- ▶ The digital LDO output is 1.8V and is required for the Cortex-M3 and other digital peripherals to operate properly.
- ▶ In the failing cases, this 1.8V rail did not come up properly and led to the Cortex-M3 never executing user code



Verification

▶ ATE Verifications Complete: No Issues

▪ **Purpose:**

- To ensure new silicon performance matches previous revision
- Tested 30x ADuCM320 devices with the ATE production test program at -40C, 25C, 85C
- Also tested 30x ADuCM310 devices with the ATE production test program at -40C, 25C, 105C

▶ Bench Verifications Complete: No Issues

- Power-On reset verification testing completed

▪ **Purpose:**

- To verify silicon change fixed previous Power-on reset issue
- Tested 3x ADuCM310's, 3x ADuCM320s
 - No ADuCM320i parts were tested (the digital die is common with ADuCM310)
 - Test involved Power cycling parts with random VDD ramp rates from 0.15mS to 750mS
 - All tests repeated in gradual sweep covering all temperatures between -40C to 125C
 - Typically >50,000 tests per unit (total of 528,000 tests)